METHOD FOR PACKAGING INTEGRATED CIRCUIT CHIPS

ABSTRACT OF THE DISCLOSURE

A method for packaging integrated circuits in a wafer format that eliminates wire bonds. A wafer substrate on which the integrated circuits have been fabricated is patterned and etched to form signal and ground via through the substrate. A back-side ground plane is deposited in contact with the ground vias. A protective layer is formed on the top surface of the substrate, and a protective layer is formed on the bottom surface of the substrate, where the bottom protective layer fills in removed substrate material between the integrated circuits. Vias are formed through the bottom protective layer, and the wafer substrate is diced between the integrated circuits.